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10/075,289	02/15/2002	Sylvie Lesmanne	T2147-907715	9018

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EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	8

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,289	LESMANNE ET AL.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated January 16, 2004. The applicant's remarks and amendment were considered with the results that follow.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on February 15, 2002 has been received and considered. Please see attached PTO-1449.

Specification

3. Claims 1-12 are presented for examination.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ekanadham et al. (USPN: 6,085,295), hereinafter Ekanadham.

As per claim 1, Ekanadham discloses in FIG. 1 a coherence controller connected to multiprocessors (PN) within a local module (NODE N), the multiprocessor (PN)

including a local main memory (MN) and a plurality of processors (PN) each equipped with a cache memory (column 2, lines 25-26 *"...remote line is brought into the cache of a processor..."*), the coherence controller comprising:

- a cache filter directory (embedded within adapter "A") including a first filter directory for guaranteeing coherence between the local main memory (MN) and the cache memory in each of the processors of the local module (NODE N) [(Ekanadham, FIG. 4, column 1, lines 35-37 *"The adapter maintains a directory of all nodes..."* and column 3, lines 57-64 *"FIG. 4 illustrates... It comprises a set of node lists **41** and local... cached by the local processors."*)];
- a complementary filter directory (embedded within adapter "A") for tracking locations of lines or blocks of the local main memory copied from the local module into at least one external module and for guaranteeing coherence between the local main memory and the cache in each of the processors of the local module and said at least one external module [(Ekanadham, FIG. 4, column 1, lines 35-37 *"The adapter maintains a directory of all nodes..."* and column 3, lines 57-64 *"FIG. 4 illustrates... It comprises a set of node lists **41** and local... cached by the local processors."*)]; and an
- external port connected to said at least one external module [(Ekanadham, FIG. 1, element A)].

As per claim 2, Ekanadham discloses in FIG. 4 the cache filter directory includes: an "n"-bit presence vector (42) where n is a number of multiprocessors in the local module, an "n-1"-bit extension of the presence vector (41), where n-1 is a total number of external modules connected to the external port, and an Exclusive status bit (43) [(Ekanadham, FIG. 4, column 3, lines 59-64 *"It comprises... node lists **41**... processor lists **42**... 2-bit line state directory **43**..."*)].

As per claim 3, Ekanadham discloses in FIG. 1 the external port (A) is connected directly or indirectly to the external modules (NODE N) via an external two-point link (NETWORK).

As per claim 4, Ekanadham discloses in FIG. 1 a coherence controller further comprising: "n" control units connected to the "n" multiprocessors in the local module (NODE N), a control unit XPU connected to the external port (embedded within adapter A), and a common control unit containing the cache filter directory (FIG. 4) [(Ekanadham, column 1, lines 59-62 *"Each processor communicates... via the switch"* and column 2, lines 52-55 *""When a memory command is issued from... a node to a memory of another node, the command is directed to an adapter...*). Note that all controlling units within claim 4 are embedded within adapter "A"].

As per claim 5, Ekanadham discloses that the control unit XPU and the "n" control units are compatible with one another and use similar protocols [(Ekanadham, column 3, lines 39-41 *"...the adapter uses the local SMP coherence protocol..."*)].

As per claim 6, Ekanadham discloses in FIG. 1 a multiprocessor module (e.g. NODE 1) connected to a coherence controller [(NODE 1 is connected to adapter "A" via a switch device "SWITCH")].

As per claim 7, Ekanadham discloses in FIG. 1 a multiprocessor system with a multimodule architecture, comprising: at least two multiprocessor modules (NODE 1 – NODE 3) connected to one another through external ports (A) of coherence controllers located within said at least two multiprocessor modules.

As per claim 8, Ekanadham discloses in FIG. 1 the external ports (A) are connected to one another through a switching device or router (NETWORK).

As per claim 9, Ekanadham discloses in FIG. 1 a switching device or a router (A) which manages and/or filters data and/or requests in transit between two multiprocessor modules (e.g. NODE 1 and NODE 2) [(Ekanadham, Column 49-55 *"The adapter connects to the switch... behaves as proxy processor..."*)].

As per claim 10, Ekanadham discloses in FIG. 1 a multimodule architecture, comprising:

- a plurality of multiprocessor modules (NODE N) wherein the multiprocessor modules include:
  - a plurality of multiprocessors (PN) each equipped with at least one cache memory and at least one local main memory, and a local coherence controller (A) connected to the multiprocessors and including a local cache filter directory (FIG.1 element A and FIG. 4), for guaranteeing local coherence between the local main memory (MN) and the cache memories in each of the multiprocessors (column 2, lines 25-26 *"...remote line is brought into the cache of a processor..."*), said local coherence controller connected to at least a second one of said multiprocessor modules (FIG.1, NODEN), wherein the coherence controller further includes:
    - a complementary cache filter directory for tracking a location of memory lines or blocks copied from said first multiprocessor module (NODE 1) to the second one (NODE 2) of the multiprocessor modules and for guaranteeing coherence between the local main memory (MN) and the cache memories in each of the multiprocessors in the first module (NODE 1) and the second one (NODE 2) of the multiprocessor modules (NODE N) [(Ekanadham, FIG. 4, column 1, lines 35-37 *"The adapter maintains a directory of all nodes..."* and

column 3, lines 57-64 *"FIG. 4 illustrates... It comprises a set of node lists **41** and local... cached by the local processors."*)].

As per claim 11, Ekanadham discloses a multimodule architecture, wherein the coherence controller includes: an "n"-bit presence vector (42) which indicates presence or absence of a copy of a memory block or line in the cache memories of the multiprocessors, an "n-1"-bit extension of the presence vector (41) which indicates presence or absence of a copy of a memory block or line in cache memories of multiprocessors in the second one of said multiprocessor modules, and an Exclusive status bit (43) [(Ekanadham, FIG. 4, column 3, lines 59-64 *"It comprises... node lists **41**... processor lists **42**... 2-bit line state directory **43**..."*)].

As per claim 12, Ekanadham discloses in FIG. 1 a multimodule architecture further comprising: switching device or router (A) which connects the first multiprocessor module (NODE 1) with the second one (NODE 2) of the multiprocessor modules (NODE N), the switching device or router (A) including a unit which manages and/or filters data and/or requests in transit between the first multiprocessor module and the second one of said multiprocessor modules [(Ekanadham, Column 49-55 *"The adapter connects to the switch... behaves as proxy processor..."*)].

Response to Arguments

6. Applicant's arguments filed January 16, 2004 with respect to independent claims 1 and 10 have been fully considered but they are not persuasive.

Applicant asserted: Ekanadham fails to disclose or suggest the cache filter directory, complimentary filter directory and the underlying architecture as recited in claims 1 and 10.

Examiner respectfully traverses Applicant's remarks for the following reasons:

Ekanadham clearly discloses the coherence controller and the necessary underlying architecture for maintaining data coherency between local module (i.e., node) and external modules as claimed, comprising a cache filter directory and a complementary filter directory included within Adapter A (e.g., see Figure 1-4). Figure 2 depicts a local cache filter directory (26), which is stored in memory M to keep track of the processors within the node that have cached copies, thus guaranteeing local data coherency within the node (e.g., *"In a switch-based SMP, the memory M maintains a directory 26. For each line 25 the directory keeps a list 24-x of the processors within the node that have cached copies of the line..."* column 1, lines 52-58). Figures 4-5 depicts a second filter directory complementing the local cache filter directory and extending data coherency to external nodes, thus guaranteeing data coherency between the local main memory and the cache copied in each of the local processors within the node and other nodes (e.g., column 1, lines 35-37 and column 3, lines 57-64).

Therefore, the rejection of claims 1 and 10 is deemed to be proper. Ekanadha discloses each and every element recited within claims 1 and 10.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thang Ho
Art Unit 2188
April 1, 2004

Mano Padmanabhan
4/2/04

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SUPERVISORY PATENT EXAMINER
TC2188